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A library defines how certain keywords behave in your file. For now, just take it for granted that you need to have these 2 lines at the top of your file: `library ieee; use ieee.std_logic_1164.all;` Congratulations! You have created your first VHDL file. You can see the completed file here:

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Following the process keyword we see that the value PB1 is listed in brackets. This tells VHDL that this signal is sensitive to how the following 'block' will work. Effectively saying you need to perform the following if that value of PB1 changes. The process then has a 'begin' and 'end process' to identify the contents.

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